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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/505,433	IWATA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2004 and 31 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 05/31/06 has been entered.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 05/31/06 have been approved.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obvious-ness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by (as is the case here), or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of copending Application No. 10/506322. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 5 of 10/506322 discloses each and every limitation of claims 1 of the instant application. The claims avoid a statutory double patenting rejection only because the channel claimed in claim 1 (from which claim 5 depends) of the copending application may meet that claim by being formed in either a substrate, a well region, or an SOI region (note claim 1 lines 2-5 of copending Application No. 10/506322), whereas to meet claim 1 of the instant application the channel must be formed in a substrate (no substitutions allowed).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-8, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by SAKAGAMI ET AL. (5,838,041).

Sakagami et al. discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 11 formed on the semiconductor substrate 1; a single gate electrode 13, said single gate electrode 13 formed on the gate insulating film 11; two charge holding portions 19 formed on the sidewalls on opposite sides of the single gate electrode 13; two diffusion layer regions 20,21 corresponding to the two charge holding portions 19 respectively; and, a channel region (marked as part #8 in prior art figure 1, but part of the disclosed invention) placed beneath the single gate electrode 13, wherein the charge holding portions 19 have a structure such that a first insulator film 17, including a portion that extends approximately parallel to sides of the gate electrode 13, having a function of holding charge is sandwiched between a

second insulator film 14 separating the semiconductor substrate 1 and the sidewalls of the gate electrode 13 from the first insulator film 17, and a third insulator film 18, and the charge holding portions 19 extend to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions 20,21 such that the amount of current flowing between one of the diffusion layer regions 20,21 and the other of the diffusion layer regions 20,21 at the time of application of a voltage to the gate electrode 13 is detected as being an indication of the quantity of charge held in the first insulator film 17, that the first insulator film 17 is of silicon nitride, and the second insulator film 14 and third insulator film 18 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 17, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator film 14, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator film 18, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 17, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the

second insulator film 14, and the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator film 18, wherein the thickness of the film made of the second insulator film 14 in the vicinity of the sidewalls of the gate electrode 13 is greater than the thickness of the film made of the second insulator film 14 on the semiconductor substrate 1; at least a portion of the first insulator film 17 overlaps a portion of the diffusion layer regions 20,21; the first insulator film 17 includes a portion having a surface approximately parallel to the surface of the gate insulating film 11, the second insulator-film thickness (being 2-10 nm, note column 4 line 64 and column 5 line 1) is no less than 1.5 nm and no greater than 15 nm, the first insulator-film thickness (being 0.5-7 nm, note column 5 lines 22-26) is no less than 2 nm and no greater than 15 nm, and the two diffusion regions 20,21 are respectively offset relative to edges of the single gate electrode 13. Note figures 2, 7, column 4 lines 6-35, and column 5 lines 30-35 of Sakagami et al.

B. Claims 1-7,9,10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by YOSHIKAWA (6,335,554).

Yoshikawa discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 2, having a gate insulating film thickness (2-25 nm, note column 7 line 36), formed on the semiconductor substrate 1; a single gate electrode 3, said single gate electrode 3 formed on the gate insulating film 2; two charge holding portions 4a-b formed on the sidewalls on opposite sides of the single gate electrode 3; two diffusion layer regions 10 corresponding to the two charge holding

portions 4a-b respectively; and a channel region placed beneath the single gate electrode 3, wherein the charge holding portions 4a-b have a structure such that a first insulator film 6, having a first insulator film thickness (10-100 nm, note column 7 line 51) including a portion that extends approximately parallel to sides of the gate electrode 3, having a function of holding charge is sandwiched between a second insulator film 5, having a second insulator film thickness (10 nm, note column 7 line 49), separating the semiconductor substrate 1 and the sidewalls of the gate electrode 3 from the first insulator film 6, and a third insulator film 7, and the charge holding portions 4a-b extend to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions 10 such that the amount of current flowing between one of the diffusion layer regions 10 and the other of the diffusion layer regions 10 at the time of application of a voltage to the gate electrode 3 is detected as being an indication of the quantity of charge held in the first insulator film 6, that the first insulator film 6 is of silicon nitride, and the second insulator film 5 and third insulator film 7 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 6, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator

film 5, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator film 7, the Φ1 represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 6, the Φ2 represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator film 5, and the Φ3 represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator film 7, wherein the second insulator film thickness in the vicinity of the sidewalls of the gate electrode 3 is greater than the second insulator film thickness on the semiconductor substrate 1, at least a portion of the first insulator film 6 overlaps a portion of the diffusion layer regions 10, the first insulator film 6 further includes a portion having a surface approximately parallel to the surface of the gate insulating film 2, the second insulator film thickness (10 nm, note column 7 line 49) is no less than 1.5 nm and no greater than 15 nm, the first insulator film thickness (10-100 nm, note column 7 line 51) is no less than 2 nm and no greater than 15 nm, the second insulator film thickness (10 nm, note column 7 line 49) may be less than the gate insulating film thickness (2-25 nm, note column 7 line 36) and not less than 0.8 nm, and may be greater than the gate insulating film thickness (2-25 nm, note column 7 line 36) not greater than 20 nm, and the two diffusion regions 10 are respectively offset relative to edges of the single gate electrode 3. Note figure 6, column 6 lines 22-36, and column 7 lines 40-55 of Yoshikawa.

C. Claims 1-10,12, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by KOBAYASHI ET AL. (2003/0161192).

Kobayashi et al. discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 4, having a gate insulating film thickness (1-10 nm, note paragraph 0103), formed on the semiconductor substrate 1; a single gate electrode 5, said single gate electrode 5 formed on the gate insulating film 4; two charge holding portions 6a-6b formed on the sidewalls on opposite sides of the single gate electrode 5; two diffusion layer regions 2a-2b corresponding to the two charge holding portions 6a-6b respectively; and a channel region Ch2 placed beneath the single gate electrode 5, wherein the charge holding portions 6a-6b have a structure such that a first insulator film 6-2, having a first insulator film thickness (3.5-6.0 nm, note paragraph 0108), including a portion that extends approximately parallel to sides of the gate electrode 5, having a function of holding charge is sandwiched between a second insulator film 6-1, having a second insulator film thickness (2.5-6.0 nm, note paragraph 0107), separating the semiconductor substrate 1 and the sidewalls of the gate electrode 5 from the first insulator film 6-2, and a third insulator film 6-3, and the charge holding portions 6a-6b extend to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions 2a-2b such that the amount of current flowing between one of the diffusion layer regions 2a-2b and the other of the diffusion layer regions 2a-2b at the time of application of a voltage to the gate electrode 5 is detected as being an indication of the quantity of charge held in the first insulator film 6-

2, that the first insulator film 6-2 is of silicon nitride, and the second insulator film 6-1 and third insulator film 6-3 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 6-2, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator film 6-1, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator film 6-3, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 6-2, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator film 6-1, and the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator film 6-3, wherein the thickness of the film made of the second insulator film 6-1 in the vicinity of the sidewalls of the gate electrode 5 is greater than the thickness of the film made of the second insulator film 6-1 on the semiconductor substrate 1, the first insulator film 6-2 includes a portion having a surface approximately parallel to the surface of the gate insulating film 4, the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is no less than

1.5 nm and no greater than 15 nm, the first insulator film thickness (3.5-6.0 nm, note paragraph 0108) is no less than 2 nm and no greater than 15 nm, the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is less than the gate insulating film thickness (1-10 nm, note paragraph 0103) and not less than 0.8 nm, the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is greater than the gate insulating film thickness (1-10 nm, note paragraph 0103) not greater than 20 nm, and the two diffusion regions 2a-2b are respectively offset relative to edges of the single gate electrode 5. Note figures 1A, 1B, and paragraphs 0099-0111 of Kobayashi et al.

Response to Arguments

5. Applicant's arguments filed 05/31/2006 have been fully considered but they are not persuasive.

On page 9 of the remarks Applicant explains that new claim 1 language "charge holding portions ... overlap a portion of the respective diffusion layer regions," requires part of the charge holding portions to be above part of the diffusion layer regions, as parts of charge holding portions 61 and 62 are above parts of diffusion layer regions 17 and 18 in Applicant's figure 1. Applicant correctly points out that in Yoshikawa 4,881,108 no part of charge holding portions 108 are formed above any part of diffusion layer regions 112 or 113. For this reason it is clear that the amended claims avoid Yoshikawa 4,881,108.

On page 10 of the remarks, after pointing out that claim 1 requires that "the charge holding portions extend to an area above a portion of the channel region and overlap a

portion of the respective diffusion layer regions," Applicant contends that "To the contrary, Sakagami teaches a charge holding portion 19 that is not formed on a portion of the channel region..." However, Sakagami states, "On the channel region between an edge of the gate electrode 13 and the diffusion layer 21, a layered film [charge holding portion 19] consisting of silicon oxide films 14 and a SiN film 17 is provided." Column 4 lines 16-18.

On page 10 of the remarks Applicant goes on to contend that the charge holding portion "... does not overlap a portion of diffusion layer regions," because, according to Applicant, "Sakagami teaches a charge holding portion 19 formed entirely over a diffusion layer region(s)." However, Sakagami states, "Each of the diffusion layers 20 and 21 is formed so as to overlap with the neighbor of the lower edge portion of [charge holding portion] 19." Column 4 lines 22-24. With all due respect to Applicant's clear eye and keen sensibility, it is necessary to give Sakagami's reading of his invention precedence over Applicant's.

It is argued, at page 11 of the remarks, that "Claim 1 requires the claimed semiconductor storage device have 'a single gate electrode,' [while] to the contrary, Yoshikawa [6,335,554] teaches a semiconductor memory having two gate electrodes 3 and 8. Furthermore, gate electrodes 8 are formed on charge holding portions 4a and 4b. The single gate electrode of the claimed invention is formed on the gate insulating film. Thus, Applicants submit that Yoshikawa [6,335,554] fails to meet each and every claimed element required by claim 1." In other words, Applicants admit that Yoshikawa

6,335,554 teaches a single gate electrode 3 formed on gate insulating film 2 but Applicants claim that Yoshikawa 6,335,554 fails to teach the claimed invention because it discloses another electrode (8) not found in claim 1.

On page 12 Applicants put forth the same argument with regard to Kobayashi 2003/0161192. Applicants point out that "Unlike the present invention, Kobayashi discloses a memory gate electrode 7 as a word line, and the gate electrode 5 serving as a the control gate (see Figs. 1A and 1B)." Applicants do not deny, however, that gate electrode 5 possesses every attribute claim 1 requires of the "single gate electrode," including being formed on gate insulating film 4 and having charge holding portions 6a and 6b formed on opposite sidewalls of gate electrode 5.

However, Applicant's claim 1 begins with the words, "A semiconductor storage device comprising [emphasis added]." Transitional phrases such as "comprising" define the scope of a claim with respect to what unrecited additional components or steps, if any, are excluded from the scope of the claim.

The transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., *Mars Inc. v. H.J. Heinz Co.*, 377 F.3d 1369, 1376, 71 USPQ2d 1837, 1843 (Fed. Cir. 2004) ("like the term 'comprising,' the terms 'containing' and 'mixture' are open-ended."). *Invitrogen Corp. v. Biocrest Mfg., L.P.*, 327 F.3d 1364, 1368, 66 USPQ2d 1631, 1634 (Fed. Cir. 2003) ("The transition 'comprising' in a method claim indicates that the claim is open-ended

and allows for additional steps."); *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 229 USPQ 805 (Fed. Cir. 1986); *In re Baxter*, 656 F.2d 679, 686, 210 USPQ 795, 803 (CCPA 1981); *Ex parte Davis*, 80 USPQ 448, 450 (Bd. App. 1948) ("comprising" leaves "the claim open for the inclusion of unspecified ingredients even in major amounts"). In *Gillette Co. v. Energizer Holdings Inc.*, 405 F.3d 1367, 1371-73, 74 USPQ2d 1586, 1589-91 (Fed. Cir. 2005), the court held that a claim to "a safety razor blade unit comprising a guard, a cap, and a group of first, second, and third blades" encompasses razors with more than three blades because the transitional phrase "comprising" in the preamble and the phrase "group of" are presumptively open-ended. "The word 'comprising' transitioning from the preamble to the body signals that the entire claim is presumptively open-ended." *Id.* In contrast, the court noted the phrase "group consisting of" is a closed term, which is often used in claim drafting to signal a "Markush group" that is by its nature closed. *Id.* The court also emphasized that reference to "first," "second," and "third" blades in the claim was not used to show a serial or numerical limitation but instead was used to distinguish or identify the various members of the group. *Id.* See MPEP § 2111.03.

Because Applicants' claim 1 "comprises" a single gate electrode, it is of no significance, as far as meeting claim 1 is concerned, whether Kobayashi's and

Yoshikawa's devices contain one gate electrode or a million. As a practical matter it should be pointed out that because we are dealing with random access memories intended for use in a modern computer, any commercial embodiment of the claimed invention is more likely to have a million (four or more gates per byte of memory, in a megabyte scale RAM) gates formed on the claimed semiconductor substrate than to have only one.

It is further argued at page 12 of the remarks, that "In the present invention, the charge holding portion is formed only on sidewalls of the gate electrode. In Kobayashi, the charge storing film 6 is formed over the control gate 5, as well as in the entire region of the semiconductor substrate between control gates." However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., not being formed over the control gate or in the region of the semiconductor substrate between control gates) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
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